

What is claimed is:

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1. A storage pixel sensor disposed on a semiconductor substrate comprising:
  - a photodiode having a first terminal coupled to a first potential and a second terminal;
  - 5 a reset transistor having a first terminal coupled to the second terminal of the photodiode, a second terminal coupled to a reset reference potential that reverse biases the photodiode, and a control gate coupled to a RESET signal node;
  - 10 a photocharge integration node coupled to said first terminal of said reset transistor, said photocharge integration node comprising the control gate of a source-follower transistor, said source-follower transistor having a drain, coupled to a source-follower drain supply voltage node, and a source coupled to means for generating a bias current; and
  - 15 a capacitive storage node, coupled to the source of the source-follower transistor, comprising the input of a readout amplifier transistor having an output.
2. The storage pixel sensor of claim 1 including means for selectively pulsing said source-follower drain supply voltage node.

3. The storage pixel sensor of claim 1 wherein said readout amplifier is a second source-follower transistor having a drain coupled to a second source-follower drain supply voltage node and said capacitive storage node is a gate associated therewith.

5 4. The storage pixel sensor of claim 3 further coupled to means for selectively pulsing said second source-follower drain supply voltage.

5. The storage pixel sensor of claim 1 wherein said means for generating a bias current comprises a bias transistor having a source coupled to a fixed voltage source, 10 a gate coupled to a bias voltage node and a drain coupled to the source of said source-follower transistor.

15 6. The storage pixel sensor of claim 5 wherein the gate of said bias transistor is coupled to a bias voltage node that may be selectively pulsed.

7. The storage pixel sensor of claim 1 further including a barrier transistor having first and second terminals coupled between the second terminal of the photodiode

and said first terminal of said reset transistor, said barrier transistor having a control terminal coupled to a barrier set voltage.

8. The storage pixel sensor of claim 7 wherein said reset transistor and said  
5 barrier transistor are sized so as to have substantially matched voltage thresholds.

9. The storage pixel sensor of claim 1 further comprising a transfer transistor  
disposed between said source of said source-follower transistor and the capacitive storage  
node, said transfer transistor having a first terminal coupled to said source of said source-  
follower transistor, a second terminal coupled to the capacitive storage node and a control  
gate coupled to a XFR signal node.  
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10. The storage pixel sensor of claim 9 further comprising:  
a row-select transistor having a first terminal coupled to the output of the  
15 readout amplifier, a second terminal coupled to a column output line and a control gate  
coupled to a ROW SELECT signal node; and

a control circuit for selectively activating a RESET signal on said RESET signal node, a XFR signal on said XFR signal node, and a ROW SELECT signal on said ROW SELECT signal node.

5        11. The storage pixel sensor of claim 1 further including an exposure transistor having a source coupled to said output of said source-follower transistor and drain coupled to a global current-summing node, said exposure transistor having a control gate coupled to a saturation level control voltage.

10      12. A storage pixel sensor disposed on a semiconductor substrate comprising:  
                a photodiode having a first terminal coupled to a first potential and a second terminal;  
                a barrier transistor having a first terminal coupled to the second terminal of the photodiode, said barrier transistor having a second terminal and a control gate  
15      coupled to a barrier set voltage;  
                a reset transistor having a first terminal coupled to the second terminal of the barrier transistor, a second terminal coupled to a reset reference potential that reverse biases the photodiode, and a control gate coupled to a RESET signal node;

a photocharge integration node coupled to said second terminal of said barrier transistor, said photocharge integration node comprising the control gate of a source-follower transistor, said source-follower transistor having a drain, coupled to a source-follower drain supply voltage node, and a source; and

- 5            a capacitive storage node, coupled to said source of said source-follower transistor, comprising the input of a readout amplifier transistor having an output.

13.        The storage pixel sensor of claim 12 including means for selectively pulsing said source-follower drain supply voltage node.

10          14.        The storage pixel sensor of claim 12 wherein said readout amplifier is a second source-follower transistor having a drain coupled to a second source-follower drain supply voltage node and said capacitive storage node is a gate associated therewith.

- 15          15.        The storage pixel sensor of claim 14 further coupled to means for selectively pulsing said second source-follower drain supply voltage.

16. The storage pixel sensor of claim 12 wherein said means for generating a bias current comprises a bias transistor having a source coupled to a fixed voltage source, a gate coupled to a bias voltage node and a drain coupled to the source of said source-follower transistor.

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17. The storage pixel sensor of claim 16 wherein the gate of said bias transistor is coupled to a bias voltage node that may be selectively pulsed.

18. The storage pixel sensor of claim 12 wherein said reset transistor and said

10 barrier transistor are sized so as to have substantially matched voltage thresholds.

19. The storage pixel sensor of claim 12 further comprising a transfer transistor

disposed between said source of said source-follower transistor and the capacitive storage

node, said transfer transistor having a first terminal coupled to said source of said source-

15 follower transistor, a second terminal coupled to the capacitive storage node and a control

gate coupled to a XFR signal node.

20. The storage pixel sensor of claim 12 further comprising a row-select transistor having a first terminal coupled to the output of the readout amplifier, a second terminal coupled to a column output line and a control gate coupled to a ROW SELECT signal node, and

5 a control circuit for selectively activating a RESET signal on said RESET signal node, a XFR signal on said XFR signal node, and a ROW SELECT signal on said ROW SELECT signal node.

21. The storage pixel sensor of claim 12 further including an exposure transistor having a source coupled to said output of said source-follower transistor and drain coupled to a global current-summing node, said exposure transistor having a control gate coupled to a saturation level control voltage.

22. A storage pixel sensor disposed on a semiconductor substrate comprising:  
15 a photodiode having a first terminal coupled to a first potential and a second terminal;

- a reset transistor having a first terminal coupled to the second terminal of  
the photodiode, a second terminal coupled to a reset reference potential that reverse  
biases the photodiode, and a control gate coupled to a RESET signal node;
- 5        a photocharge integration node coupled to said second terminal of said  
photodiode, said photocharge integration node comprising the control gate of a source-  
follower transistor, said source-follower transistor having a drain, coupled to a source-  
follower drain supply voltage node, and a source;
- 10        a capacitive storage node, coupled to said source of said source-follower  
transistor, comprising the input of a readout amplifier transistor having an output; and  
15        an exposure transistor having a source coupled to said source of said  
source-follower transistor and drain coupled to a global current-summing node, said  
exposure transistor having a control gate coupled to a saturation level control voltage.
23.        The storage pixel sensor of claim 22 including means for selectively  
15 pulsing said source-follower drain supply voltage node.

24. The storage pixel sensor of claim 22 wherein said readout amplifier is a second source-follower transistor having a drain coupled to a second source-follower drain supply voltage node and said capacitive storage node is a gate associated therewith.

5 25. The storage pixel sensor of claim 24 further including means for selectively pulsing said second source-follower drain supply voltage.

26. The storage pixel sensor of claim 24 further including a bias transistor having a source coupled to a fixed voltage source, a gate coupled to a bias voltage node and a drain forming said means for generating a bias current and coupled to the source of said source-follower transistor.

10 15 27. The storage pixel sensor of claim 26 wherein the gate of said bias transistor is coupled to a bias voltage node that may be selectively pulsed.

28. The storage pixel sensor of claim 22 wherein said reset transistor and said barrier transistor are sized so as to have substantially matched voltage thresholds.

29. The storage pixel sensor of claim 22 further comprising a transfer transistor disposed between said source of said source-follower transistor and the capacitive storage node, said transfer transistor having a first terminal coupled to said source of said source-follower transistor, a second terminal coupled to the capacitive storage node and a control gate coupled to a XFR signal node.

30. The storage pixel sensor of claim 22 further comprising a row-select transistor having a first terminal coupled to the output of the readout amplifier, a second terminal coupled to a column output line and a control gate coupled to a ROW SELECT signal node, and

a control circuit for selectively activating a RESET signal on said RESET signal node, a XFR signal on said XFR signal node, and a ROW SELECT signal on said ROW SELECT signal node.

15 31. A storage pixel sensor disposed on a semiconductor substrate comprising:

a photodiode having a first terminal coupled to a first potential and a second terminal;

- a reset transistor having a first terminal coupled to the second terminal of  
the photodiode, a second terminal coupled to a reset reference potential that reverse  
biases the photodiode, and a control gate coupled to a RESET signal node;
- 5        a photocharge integration node coupled to said second terminal of said  
photodiode, said photocharge integration node comprising the control gate of a source-  
follower transistor, said source-follower transistor having a drain, coupled to a source-  
follower drain supply voltage node, and a source;
- 10        a capacitive storage node, coupled to said source of said source-follower  
transistor, comprising the input of a readout amplifier transistor having an output; and
- 15        a transfer transistor disposed between said source of said source-follower  
transistor and the capacitive storage node, said transfer transistor having a first terminal  
coupled to said source of said source-follower transistor, a second terminal coupled to the  
capacitive storage node and a control gate coupled to a XFR signal node.
32.      The storage pixel sensor of claim 30 including means for selectively  
pulsing said source-follower drain supply voltage node.

33. The storage pixel sensor of claim 30 wherein said readout amplifier is a second source-follower transistor having a drain coupled to a second source-follower drain supply voltage node and said capacitive storage node is a gate associated therewith.

5 34. The storage pixel sensor of claim 33 further including means for selectively pulsing said second source-follower drain supply voltage.

35. The storage pixel sensor of claim 30 further including a bias transistor having a source coupled to a fixed voltage source, a gate coupled to a bias voltage node 10 and a drain forming said means for generating a bias current and coupled to the source of said source-follower transistor.

36. The storage pixel sensor of claim 35 wherein the gate of said bias transistor is coupled to a bias voltage node that may be selectively pulsed.

15 37. The storage pixel sensor of claim 30 wherein said reset transistor and said barrier transistor are sized so as to have substantially matched voltage thresholds.

38. The storage pixel sensor of claim 30 further comprising a row-select transistor having a first terminal coupled to the output of the readout amplifier, a second terminal coupled to a column output line and a control gate coupled to a ROW SELECT signal node, and

5 a control circuit for selectively activating a RESET signal on said RESET signal node, a XFR signal on said XFR signal node, and a ROW SELECT signal on said ROW SELECT signal node.

39. A pixel sensor disposed on a semiconductor substrate comprising:

10 a photodiode having a first terminal coupled to a first potential and a second terminal;

a reset transistor having a first terminal coupled to the second terminal of the photodiode, a second terminal coupled to a reset reference potential that reverse biases the photodiode, and a control gate coupled to a RESET signal node;

15 a photocharge integration node coupled to said first terminal of said reset transistor, said photocharge integration node comprising the control gate of a source-follower transistor, said source-follower transistor having a drain coupled to a source-

follower drain supply voltage node and a source coupled to means for generating a bias current; and

an exposure transistor having a source coupled to said output of said source-follower transistor and drain coupled to a global current-summing node, said 5 exposure transistor having a control gate coupled to a saturation level control voltage.

40. The pixel sensor of claim 39 further coupled to means for selectively pulsing said source-follower drain supply voltage node.

10 41. The pixel sensor of claim 39 wherein said means for generating a bias current comprises a bias transistor having a source coupled to a fixed voltage source, a gate coupled to a bias voltage node and a drain coupled to the source of said source-follower transistor.

15 42. The pixel sensor of claim 41 wherein the gate of said bias transistor is coupled to a bias voltage node that may be selectively pulsed.

43. The pixel sensor of claim 39 further including a barrier transistor having first and second terminals coupled between the second terminal of the photodiode and said first terminal of said reset transistor, said barrier transistor having a control terminal coupled to a barrier set voltage.

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44. The pixel sensor of claim 43 wherein said reset transistor and said barrier transistor are sized so as to have substantially matched voltage thresholds.

45. The pixel sensor of claim 39, further including a capacitive storage node,

10 coupled to said source of said source-follower transistor, comprising the input of a readout amplifier transistor having an output.

46. The storage pixel sensor of claim 45 wherein said readout amplifier is a

second source-follower transistor having a drain coupled to a second source-follower  
15 drain supply voltage node and said capacitive storage node is a gate associated therewith.

47. The storage pixel sensor of claim 46 further including means for selectively pulsing said second source-follower drain supply voltage.

48. The storage pixel sensor of claim 46 further comprising a transfer transistor disposed between the output of the source-follower transistor and the capacitive storage node, said transfer transistor having a first terminal coupled to the output of the source-follower transistor, a second terminal coupled to the capacitive storage node and a control gate coupled to a XFR signal node.

49. The storage pixel sensor of claim 48 further comprising:

a row-select transistor having a first terminal coupled to the output of the readout amplifier, a second terminal coupled to a column output line and a control gate coupled to a ROW SELECT signal node; and

a control circuit for selectively activating a RESET signal on said RESET signal node, a XFR signal on said XFR signal node, and a ROW SELECT signal on said ROW SELECT signal node.